AMENDMENTS TO THE CLAIMS

1. (CURRENTLY AMENDED) An apparatus comprising:

an input circuit configured to generate a plurality of data paths in response to an input data signal having a plurality of data items sequentially presented in a first order;

a storage circuit configured to store each of said data paths in a respective shift register chain; and

an output circuit configured to generate an output data signal in response to each of said shift register chains, wherein (i) said output data signal presents said data items in a second order different from said first order and (ii) a first group of said shift register chains having a first number of registers is configured to have a first delay and a second group of said shift register chains having a second number of registers different from said first number of registers is configured to have a second delay.

2. (ORIGINAL) The apparatus according to claim 1, wherein said first order comprises a sequential presentation of said plurality of data items.

3. (ORIGINAL) The apparatus according to claim 1, wherein said second order comprises a sequential presentation of said plurality of data items.

4. (ORIGINAL) The apparatus according to claim 1, wherein said input circuit comprises a demultiplexer circuit.

5. (ORIGINAL) The apparatus according to claim 1, wherein said output circuit comprises a multiplexer circuit.

6. (ORIGINAL) The apparatus according to claim 1, wherein said input circuit is controlled by a finite state machine.

7. (PREVIOUSLY PRESENTED) The apparatus according to claim 6, wherein said output circuit is controlled by said finite state machine.

8. (ORIGINAL) The apparatus according to claim 1, wherein each of said data paths is configured to have a propagation delay.

9. (CURRENTLY AMENDED) An apparatus comprising:

means for generating a plurality of data paths in response to an input data signal having a plurality of data items sequentially presented in a first order;

means for storing each of said data paths in a respective shift register chain; and

means for generating an output data signal in response to each of said shift register chains, wherein (i) said output data signal presents said data items in a second order different from said first order and (ii) a first group of said shift register chains having a first number of registers is configured to have a first delay and a second group of said shift register chains having a second number of registers different from said first number of registers is configured to have a second delay.

10. (CURRENTLY AMENDED) A method for re-ordering data comprising the steps of:

(A) generating a plurality of data paths in response to an input data signal having a plurality of data items sequentially presented in a first order;

(B) storing each of said data paths in a respective shift register chain; and

(C) generating an output data signal in response to each of said shift register chains, wherein (i) said output data signal presents said data items in a second order different from said

first order and (ii) a first group of said shift register chains having a first number of registers is configured to have a first delay and a second group of said shift register chains having a second number of registers different from said first number of registers is configured to have a second delay.

11. (ORIGINAL) The method according to claim 10, wherein said first order comprises a sequential presentation of said plurality of data items.

12. (ORIGINAL) The method according to claim 10, wherein said second order comprises a sequential presentation of said plurality of data items.

13. (ORIGINAL) The method according to claim 10, wherein step (A) generates said data paths using a finite state machine.

14. (ORIGINAL) The method according to claim 13, wherein step (C) generates said output data signal using said finite state machine.

15. (PREVIOUSLY PRESENTED) The method according to claim 10, wherein each of said data paths is configured to have a propagation delay.

16. (CURRENTLY AMENDED) An apparatus comprising:

an input circuit configured to generate a plurality of data paths in response to an input data signal having a plurality of data items sequentially presented in a first order;

a storage circuit configured to store each of said data paths in a memory; and

an output circuit configured to generate an output data signal in response to said memory, wherein (i) said output data signal presents said data items in a second order different from said first order and (ii) a first group of said paths having a first number of registers is configured to have a first delay and a second group of said paths having a second number of registers different from said first number of registers is configured to have a second delay.

17. (PREVIOUSLY PRESENTED) The apparatus according to claim 1, wherein said first delay is generated in response to a first particular number of shift registers and said second delay is generated in response to a second particular number of shift registers.